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Docket No.: NL 010013

TO: Examiner: CHEN, Tse W.

Art Unit: 2116

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Appeal Brief (in triplicate) – 9 pages

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Coenen**
Application No.	:	**10/042,464**
Filed	:	**January 11, 2002**
For	:	**POWER MANAGEMENT FOR DIGITAL PROCESSING APPARATUS**

APPEAL BRIEF

On Appeal from Group Art Unit 2116

Date: August 22, 2005

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

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Daniel Michalek
(Name)

22-Aug-05.
(Signature and Date)

TABLE OF CONTENTS

TABLE OF CASES

NONE

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-10 have been presented for examination. All of these claims are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to power management for a digital processing apparatus. As recited in claim 1, for example, a plurality of sub-clocking signals change from a power-up rest condition to a *free running condition* one at a time following an

initial switch-on of a digital processing apparatus. The free running nature of the sub-clocks is illustrated in Figure 2 of the specification, for example.

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 1-10 are anticipated by Smentek.

VII. ARGUMENT

I. Rejection of Claims 1-10 as anticipated by Smentek

In Smentek, signals FIRE1-FIRE8 are generated sequentially. These signals are "single-shot" signals as illustrated in Figure 2 of Smentek; they are not *free running* sub-clocks as in the present invention.

The Final Rejection tries to minimize this difference by pointing out that the claims do not require that the sub-clocks be *continuously* free-running. Applicant does not dispute this point. However, to call the single-shot signals of Smentek free-running would contradict the meaning of that term as it is understood by those of ordinary skill in the art.

Accordingly, Smentek cannot be said to anticipate the invention recited in claims 1 and 2.

With regard to dependent claims 2-10, these claims depend from independent claim 2, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claims.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings fail to anticipate the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: August 22, 2005

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A method of power management in a digital processing apparatus, the method comprising:

receiving a free-running master clock signal; and

generating a plurality of sub-clocking signals from said master clock signal, wherein said plurality of sub-clocking signals change from a power-up rest condition to a free running condition one at a time, following an initial switch-on of said digital processing apparatus (30).

2. A device for power management in a digital processing apparatus, the device comprising:

means (10, 20) for receiving a free-running master clock signal; and

means (10, 20) for generating a plurality of sub-clocking signals from said master clock signal, wherein said plurality of sub-clocking signals change from a power-up rest condition to a free running condition one at a time, following an initial switch-on of said digital processing apparatus (30).

3. A device according to claim 2, wherein each sub-clocking signal is used to clock a separate data processing part (30_0-30_3) of said apparatus (30).

4. A device according to claim 2, wherein each data processing part (30_0-30_3) comprises circuitry for processing a particular serial data bit or bits of a data word.

5. A device according to claim 4, wherein said digital signal processing apparatus has a particular maximum data width and wherein said plurality of sub-clocking signals corresponds to said maximum data width.

6. A device according to claim 2, wherein during a switch-off phase of said digital processing apparatus, said plurality of sub-clocking signals change from a free

running condition to a rest condition one at a time.

7. A device according to claim 2, wherein said means for receiving a master clocking signal and generating a plurality of sub-clocking signals comprise:

a shift register (10) for providing a plurality of enabling signals, said plurality of enabling signals each changing from a non-active rest condition to an active normal condition and thereafter remaining at said active normal condition, said plurality of enable signals changing from the rest condition to the normal condition one at a time at predetermined time intervals following the initial switch on; and

logic circuitry (20) for receiving the enable signals and sequentially enabling the production of the sub-clocking signals.

8. A device according to claim 7, wherein the logic circuitry (20) comprises means (20_0-20_3) for ANDing respective enable signals with the master clock.

9. A device according to claim 8, wherein the logic circuitry (20) comprises a number of AND gates (22_0-22_3) corresponding to the number of enable signals, each AND gate (22_0-22_3) having a first input (24_0-24_3) for receiving its respective enable signal and a second input (26_0-26_3) for receiving the master clocking signal, said sub-clocking signals being produced at the respective outputs of said AND gates.

10. Digital processing apparatus comprising:

a device in accordance with claim 2, and

a plurality of discrete data processing parts, each of said data processing parts being clocked by a respective one of said plurality of sub-clocking signals.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE

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